Advanced Research in Electrical and Electronic Engineering
Print ISSN: 2349-5804; Online ISSN: 2349-5812 Volume 2, Number 4 January-March (2015) pp. 307-312
© Krishi Sanskriti Publications
http://www.krishisanskriti.org/areee.html

FinFET: An Evolution in Structure of Planar Bulk Devices

Anterpreet Gill[1], Charu Madhu[2] and Pardeep Kaur[3]

[1,2,3]Department of Electronics and Communication University Institute of Engineering Technology Panjab University, Chandigarh, India
E-mail: [1]gillpreetanter@gmail. com

Abstract—*This paper deals with detailed description about the different technologies, which have emerged as the most candidates to extend Complementary metal oxide semiconductor (CMOS) technology beyond its scaling limits and provide a key for continuous growth of silicon-based semiconductor industry. As the scaling down of device dimension enters into nanometer regime, CMOS devices face many undesirable problems. One of them is short channel effect. To overcome these problems, researchers have innovated various CMOS materials and different nanoelectronic device structures have been introduced over the past three decades. Multigate device is emerged as the most promising candidate, which is being investigated for the improvement of conventional CMOS devices. FinFET is a multigatedevice, which is capable of controlling leakage current and reduce the short channel effect thus produce a strong drive current. FinFET has better electrostatic control than the conventional planar FET, resulting in higher density, lower power, and higher performance. This paper provides information about different emerging technologies in microelectronic industry to extend the scaling limits and highlights short channel effects.*

Keyword: *FinFET, CMOS, Multigate, Scaling, Nano electronics, Short Channel Effects*

1. INTRODUCTION

The invention of CMOS has provided a sea change in VLSI industry. It has become a prime building block in electronic industry. Its constantly increasing use in electronics item (mobile,computer,etc.) has not only boost the progress of electronic industry but has also gained the attention of researchers to develop more and more compact size devices with better performances. So the microelectronics industry has importantly invested in new and better technologies targeting at the fabrication of devices with extremely reduced dimensions. This has given rise to the design of different types of MOSFET with the target to improve the characteristics of the device[1,2].

Todays, the main aim of electronic industry is scaling down the dimension of devices to get reduced sizes and fast switching speed, which results in shrinking the dimensions of MOS transistors. As the scaling of devices reach to submicron region, an undesirable phenomenon occurs i. e. short channel effects, which prevents further scaling. These give rise to leakage current, threshold voltage roll off, higher subthreshold slope, which degrades the performance of device. The solution to this problem is multigate transisitors for example double gate MOSFET, FinFET [3]. Because of their structure, they have better control of gate over the channel, which results in reduction in leakage current. In addition, Multigate devices provide devices in nano dimension and with improved performance.

2. REASON FOR MOSFET SCALING

There are mainly two reasons for scaling down of devices. The first reason to make transistor reduce in size is to pack more and more devices in a given chip area which results in improved functionality for the same chip area[4]. It also provide lower cost per chip because in VLSI industry, fabrication cost per integrated circuits depends upon the number of chips per wafer. Hence, more number of chips per wafer can be developed with smaller IC's and reduced cost. The technique of scaled down of devices to get more devices packed in given chip area was first discovered by Gorden Moore in 1965 and named it as Moore's law which states that the number of transistors doubles every 2-3 years for same chip[5]. The second reason of scaling is to increase the switching speed. The main dimension of the device are channel length, channel width and oxide thickness. If all these device dimensions are scale down by an equal factor, there will be no change in channel resistance but channel capacitance will be reduces by same factor. So when all device dimensions are reduced proportionally, RC delay of device is reduced by similar factor. Hence, it increases the switching speed of device. But this is a case for older technologies. For toady's generation of device, scaling down of device dimensions does not necessarily translate to higher chip speed[4].

3. SHORT CHANNEL EFFECTS

In electronics, a short-channel effect is defined as an effect occurs in MOSFET when the channel length of MOSFET and depletion layer widths of source and drain junction are of same order of magnitude, which cause the characteristic of MOSFET different from other MOSFETs. This happens when electronic devices are scaled down to get increased switching speed and more number of transistors per chip [6]. The short channel effects mainly cause two phenomenons in MOSFET:

a. It cause limitation on electron drift characteristic in the channel
b. Shrinking of channel length cause variation in threshold voltage.

Shrinking in device dimension leads to problem in planer or bulk Si CMOS technology. Various short channel effects like increase in leakage current, drain induce barrier lowering, hot carrier effects, impact ionization etc. get produced in device and affect the device characteristic[7].

The aim of this paper is to provide information about different short channel effects and introduce many new technologies emerging in microelectronics industry which broad the scaling limits[4]. Drain induce barrier lowering is defined as a short channel effect in which there is a reduction of threshold voltage on increasing drain voltage. So, it is basically lowering of potential barrier of channel on increasing drain voltage. Planar field effect transistor have channel length long enough to provide electrostatic shielding from drain by the combination of gate and substrate so their threshold voltage does not depend on drain voltage but in case of short channel devices, the drain is close to gate due to which the p-n junction of drain and substrate extends under the gate when the drain voltage is large which results in attraction of more carrier into the channel [7]. Due to this, potential barrier of channel reduces which lead to turn on of device prematurely. This phenomenon is known as DIBL. The reduction in barrier voltage increases as the channel length is reduced even when the applied drain voltage is zero. This happens because of formation of depletion layers of p-n junction of source and drain with body.

There is also affect of DIBL on current VS drain bias curve in the active mode. Due to DIBL the current in active mode increases when there is an increase in drain voltage. This results in reduction of output resistance.

The other short channel effect is impact ionization. It is a phenomenon in which high velocity of electrons generate electron-hole (e-h) pairs by striking and ionizing the Si atoms in the presence of high electric field. In this process the electrons are attracted by drain and some holes enter the substrate region and produce a part of parasitic current. If a voltage drop of 0. 6V in substrate material is caused by hole current which is produced due to collection of holes by source, then there will be conduction because of formation of reverse biased substrate source p-n junction. This process of MOSFET is similar to npn transistor where channel act as base, source as emitter, and drain as collector. The electrons gain enough energy on moving towards drain to cause the formation of e-h pairs. Impact ionization can also affect the device if electrons having high kinetic energy penetrate into the substrate, escaping from the drain field.

“Hot Carrier Injection” is a short channel effect, which is described as a process of injection of carriers into the gate dielectric from the conducting channel of substrate. This causes the trapping of charge carrier in gate dielectric, which changes the switching characteristic of device. The process of creation of hot carrier happens when an electron of conducting channel jump out of the valence band to the conduction band on receiving a energy from high energy photon of electromagnetic radiation that strike the semiconductor. This transformation of energy from photon to electron generates electron hole pairs. The electron that leaves the valence band and jump to conduction band becomes the “hot electron”. These are called hot electrons because they are characterized by high effective temperature. Hot carriers have the property of high mobility and affect the reliability of semiconductor. Supply voltage is also an important parameter of scaling process but there is a limit of supply voltage to which device can be scaled, because as supply voltage is increased, high electric field is produced which cause generation of high energy carriers i. e. hot carriers. These high- energy carriers possibly penetrate into the dielectric films, oxides and gate material. Velocity saturation is also a type of short channel effect. Saturation velocity means a velocity that reaches a maximum value on applying high electric field in a semiconductor and this state of semiconductor is known as velocity saturation. The average drift speed of carrier directly depends on the electric field strength and the dependent constant is known as mobility of carrier. The mobility differs from material to material so for good conductor the mobility of charge carrier is high. Higher the mobility means higher velocity which results in higher drain current values for a given electric field strength. But because of saturation velocity, drain current does not change after some electric field value. This happens because charge carrier loose energy by interacting with silicon atoms when electric filed is increased and the emit phonons and photons. So tis mechanisms limits the movement of charge carrier in the material and so the drain current[7].

4. DIFFERENT TECHNIQUES TO EXTEND MOS SCALING

As the MOSFET channel length is scaled down to submicron region i. e. 50nm and below, the control of gate over channel decreases and also over switching of MOSFET The Scaling results in an undesirable off-state leakage current that prevent the further scaling of the conventional MOSFET structure. So

to extend MOS scaling beyond bulk limits different techniques were introduced. One of them is high doping concentration of MOSFET body, which is required to control short channel effects[8]. Using this method the traditional bulk MOSFET can be scale down to 10 nm length regime. But high doping density results in lowering of carrier mobility due to impurity scattering and an increased transverse electric field. Moreover, depletion charge is formed in channel that results in increase in average vertical filed. Increase in depletion charge also lead to large depletion capacitance and subthreshold slope. So for specific off-state leakage current, the value of threshold voltage must be increased which reduce the on state current[9]. The other way of MOS scaling is to introduce a heavy doped region near the both ends of channel. This heavy dopes region is called halo implant or Pocket implant, which is localized to prevent the state of punch-through. Fig. 1 shows the structure of Bulk MOSFET.

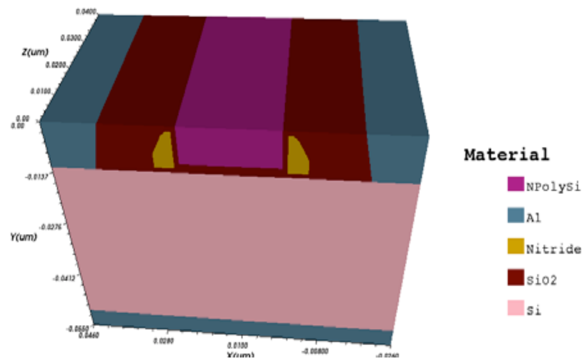


Fig. 1: Three-dimensional structure of bulk MOSFET

The other techniques to extend MOS scaling are ultra thin body devices and double gate devices. In these techniques short channel effect are controlled by formation of thin silicon film through which gate length can be scaled down to 10nm length without using channel dopants. The ultrathin body devices use a thin silicon film usually less than 20nm developed on an insulator mainly buried oxide[9,10]. The introduction of insulator in these devices is to eliminate leakage currents flow to the substrate so by introducing insulator, leakage current path from source, drain and channel to substrate is cut off. It also eliminates parasitic capacitance. The structure of UTB devices minimize the parasitic series resistance and increase drive current because of self aligned source and drain[11]. Fig. 2 shows the FDSOI structure. In both UTB and DG devices, there is lightly doped region, which shows very less depletion charge and capacitance and results in steep subthreshold slope. Addition to the low transverse electric field, these both devices shows negligible impurity scattering that give rise to high mobility and so improved drive current. For UTB devices, the gate length of 25nm and below requires body thickness below 5nm. But at this dimension the device shows degradation in performance so another technique is introduced i. e. Multigate device. Because of presence of two or more gate, multigate devices have better control over channel and thus shows reduction in short channel effects. Moreover, these devices provide additional gate length scaling[10,12].

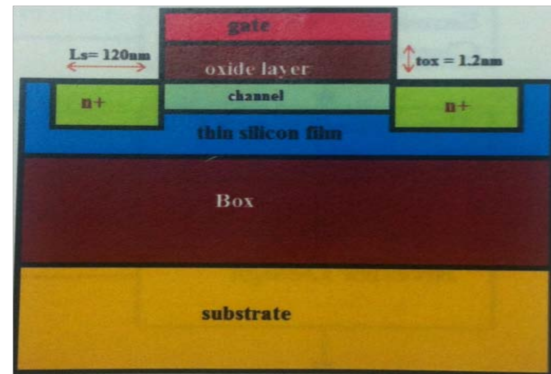


Fig. 2: FDSOI structure

Double gate device is a multigate device, which has front and back gate. The introduction of second gate reduces the body thickness effect and penetration of drain electric field to the buried oxide is also eliminated. Double gate devices are better than UTB devices because of better subthreshold slope and better short channel effect control[13]. Fig. 3 shows the double gate MOSFET structure. Table1 shows the comparison of Planar Si, Bulk Si Tri-Gate (tapered and rectangular profiles), and UTB SOI on the basis of threshold voltage, drain current and short channel effects [9]. The short channel effects are higher in Planar Si because of poor control of gate than the other two devices.

Table 1: Comparison Of Planar Si, Si Tri-Gate and UTB SOI for I_{OFF} of 100 nA/□m and at 0. 8 V V_{CC} withL_G= 26 Nm [9]

nMOS	$V_T$sat (mV)	I_{DSat} (mA/µm)	I_{DLin} (mA/µm)	SS (mV/dec)	DIBL (mV/V)
Planar Si	185	0. 678	0. 104	105	128
Tapered Si Tri-Gate	165	1. 068	0. 198	75	52
Rectangular Si tri-Gate	151	1. 155	0. 222	70	43
UTB SOI	186	1. 196	0. 202	97	89

FinFET is a multigate device, which has attained the attention of researchers among multigate devices as it shows compatibility with conventional CMOS process[14]. FinFET device consist of fin shaped structure, which is fabricated over the wafer surface. This fin is a silicon film of thickness T_{si} and it makes the source, drain and channel region of a device[15]. The fin is surrounded by top, front and back gate so the control of gate over the channel increases which results in high I_{on}/I_{off} ratio[16,17]. Moreover the thickness of film is kept low to limit the short channel effects.

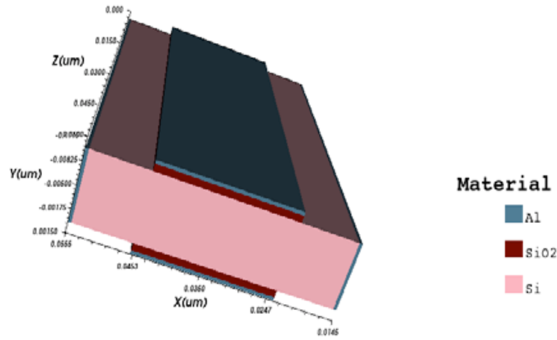


Fig. 3: Three-dimensional structure of DGFET

The effective channel length of a device is a region of a fin, which is surrounded by gates. Because of fin shaped structure this device is known as FinFET[18-25]. Fig. 4 shows the device of FinFET structure.

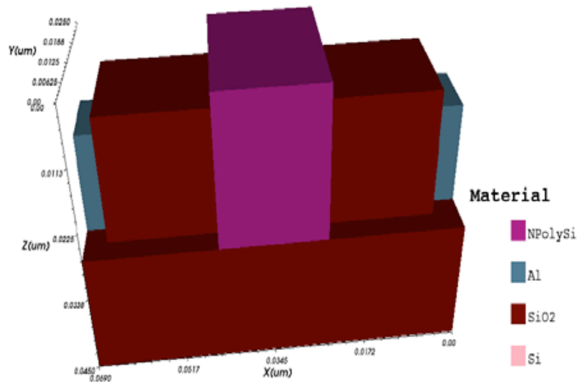
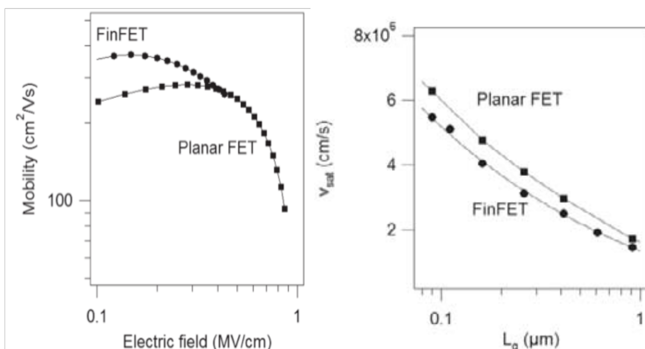


Fig. 4: Three-dimensional FinFET Structure

Fig. 5 shows the comparison of performance characteristic of Planar FET and FinFET[15]. Fig. 5(a) shows that FinFET obtained its maximum mobility at lower electric fields and is higher than Planar FET. This is because of low doping concentration in FinFET that leads to lower electric field and cause reduction in scattering, which results in higher mobility. Fig. 5(b) shows the curve between saturation velocity and gate length [15]. The saturation velocity of FinFET is lesser than planar bulk MOSFET because of lesser availabilityof volume for the movement of carrier in FinFET channel.



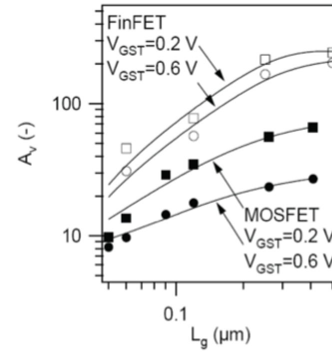


Fig. 5: Comparison of performance characteristic of FinFET and bulk MOSFET (a) mobility versus electric field (b) saturation velocity versus gate length (c) voltage gain versus gate length [15]

Fig. 5(c) shows the comparison of voltage gain of planar bulk MOSFET and FinFET [15]. The FinFET has higher voltage gain than planar bulk MOSFET.

The height of the fin cannot be greater than twice the channel length, so range of height of FinFET device is fixed. The width of FinFET is increased by adding multiple fins parallel to each other in order to increase the current or to get improved output characteristic of FinFET for different applications, [26].

The width of the FinFET device can be defined as[15]

$$W = 2H_{fin} + T_{fin} \quad (1)$$

Where H_{fin} is the fin height and T_{fin} is fin thickness. For multiple parallel fins, the width is given as [15]

$$W_{total} = n \times W_{min} = n \times (2 \times H_{fin} + T_{fin}) \quad (2)$$

Here n is number of fins.

Multiple fins are designed to increase the channel width of FinFET, which increase the drive current. Fig. 6 shows the structure of multi fin FinFET. In FinFET device, the raised structure of source and drain helps to reduce parasitic resistance so further improves drive current[26].

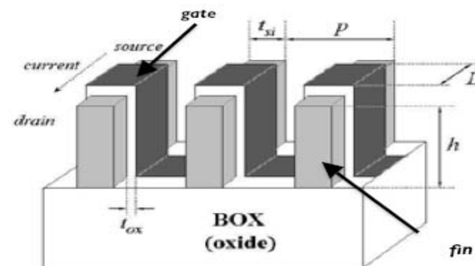


Fig. 6: Multi-fin FinFET structure [26]

An independent-gate FinFET is a type of FinFET, which is formed by depositing oxide layer on top of fin. This oxide layer separates vertical gates and form IG FinFET[27].

5. CONCLUSION

Technology scaling has provided us with increased circuit performance over the past two decades. New technologies have been emerged in microelectronics industry to reduce the problems coming in way of scaling as short channel effects. Multigate device is one of these techonolgy, which has attained the attention of researchers. FinFET has potential for reductions of the required number of transistors and chip area in circuits, which is crucial for many digital applications. It has better controlling over several short channel effects compare to the planner MOSFET. So in nanometer regime the FinFET gives better performance compare to the planner MOSFET.

6. ACKNOWLEDGEMENT

I would like to thank my guide Miss. Charu madhu, for her constant support and inspiration. I am also thankful to my co-guide Miss Pardeep Kaur, for her for advice.

REFERENCES

[1] Hutchby,J. A. , Bourianoff,G. I. , Zhirnov, V. V. and Brewer, J. E. ,“Extending the road beyond CMOS” *IEEE circuits and device magazine*,Vol:18, No. 2,pp. 28. 41, March 2002
[2] Albert Chin and Séan P. McAliste, “The power of functional scaling: beyond the power consumption challenge and the scaling roadmap” *IEEE circuits and device magazine*Vol:21, No. 1 , pp. 27-35, Jan-Feb 2005
[3] Leland Chang, Yang-Kyu Choi, Daewon Ha, Pushkar Ranade, Shiying Xiong, Jeffrey Bokor, Chenming Hu, and Tsu-Jae King, “Extremely Scaled Silicon Nano-CMOS Devices”*IEEE Transactions On Electron Devices*, Vol. 91, No. 11, pp. 1860-1873, November 2003
[4] Ali Khakifirooz and Dimitri A. Antoniadis, “MOSFET Performance Scaling—Part I: Historical Trends” *IEEE Transactions On Electron Devices*, Vol. 55, No. 6, pp. 1391-1400, JUNE 2008
[5] Chien, A. A. and Karamcheti, V. “Moore's Law: The First Ending and a New Beginning” Computer, Vol: 46, No. 12, Dec 2013.
[6] Mahender Veshala, Ramchander Jatooth, Kota and Rajesh Reddy, “Reduction of Short-Channel Effects in FinFET” *International Journal of Engineering and Innovative Technology (IJEIT)* Vol 2, No. 9,pp. 118-124, March 2013
[7] Anurag Chaudhry and M. Jagadesh Kumar, “Controlling Short-channel Effects in Deep Submicron SOI MOSFETs for Improved Reliability: A Review” *IEEE trans. on device and Materials Reliability*, Vol. 4, pp. 99-109, March 2004
[8] Xin Sun, Victor Moroz, Nattapol Damrongplasit, Changhwan Shin, and Tsu-Jae King Liu,“Variation Study of the Planar Ground-Plane Bulk MOSFET, SOI FinFET, and Trigate Bulk MOSFET Designs” *IEEE Transactions On Electron Devices*,Vol. 58, No. 10, pp. 3294-3299, October 2011
[9] Nidhi Agrawal, Yoshie Kimura, Reza Arghavani, and Suman Datta, “Impact of Transistor Architecture (Bulk Planar, Trigate on Bulk, Ultrathin-Body Planar SOI) and Material (Silicon or III–V Semiconductor) on Variation for Logic and SRAM Applications*” IEEE Transactions On Electron Devices*, Vol. 60, No. 10, pp. 3298-3304, October 2013
[10] Qian Xie, Chia-Jung Lee, Jun Xu, Wann, C. , Sun, J. Y. -C. and Yuan Taur “Comprehensive Analysis of Short-Channel Effects in Ultrathin SOI MOSFETs*”, IEEE Transactions On Electron Devices* Vol:60, No. 6, June 2013
[11] Gnani, E. , Gnudi, A., Reggiani, S. and Baccarani, G. , “Physical Model of the Junctionless UTB SOI-FET”*IEEE Transactions On Electron Devices*, Vol. 59, No. 4, April 2012
[12] Felice Crupi, Ben Kaczer, Robin Degraeve, Vaidy Subramanian, Purushothaman Srinivasan, Eddy Simoen, Abhisek Dixit, Malgorzata Jurczak, and Guido Groeseneken, “Reliability Comparison of Triple-Gate Versus Planar SOI FETs” *IEEE Transactions On Electron Devices*, Vol. 53, No. 9, pp. 2351-2357, September 2006
[13] Yiming Li and Hong-Mu Chou “A Comparative Study of Electrical Characteristic on Sub-10-nm Double-Gate MOSFETs” *IEEE Transactions On Nanotechnology*, Vol. 4, No. 5, pp. 645-647,September 2005
[14] Shiying Xiong and Jeffrey Bokor, “Sensitivity of Double-Gate and FinFET Devices to Process Variations” *IEEE Transactions On Electron Devices,* Vol. 50, No. 11,pp. 2255-2261, November 2003.
[15] Sarman K Hadia, Rohit R. PatelandDr. Yogesh P. Kosta, “FinFET Architecture Analysis and Fabrication Mechanism” *IJCSI International Journal of Computer Science Issues*, Vol. 8, Issue 5, No 1, pp. 235-240, September 2011
[16] Fasarakis, N. , Tsormpatzoglou, A. , Tassis, D. H. , Pappas, I. , Papathanasiou, K. , Bucher, M. , Ghibaudo, G. , and Dimitriadis, C. A. “Compact Model of Drain Current in Short-Channel Triple-Gate FinFETs” Electron Devices, *IEEE Transactions,* Issue: 7 , July 2012.
[17] Matteo Agostinelli, Massimo Alioto, David Esseniand Luca Selmi “Leakage–Delay Tradeoff in FinFET Logic Circuits: A Comparative Analysis With Bulk Technology” *IEEE Transactions On Very Large Scale Integration (VlSI) Systems*, Vol. 18, No. 2, February 2010
[18] Digh Hisamoto, Wen-Chin Lee, Jakub Kedzierski, Hideki Takeuchi, Kazuya Asano, Charles Kuo, Erik Anderson, Tsu-Jae King, Jeffrey Bokor and Chenming Hu, “FinFET—A Self-Aligned Double-Gate MOSFET Scalable to 20 nm” *IEEE Transactions On Electron Devices,* Vol. 47, No. 12,pp. 2320-2325, December 2000
[19] Masoud Rostami and Kartik Mohanram, “Dual-Vth Independent-Gate FinFETs for Low Power Logic Circuits” *IEEE Transactions On Computer-Aided Design Of Integrated Circuits And Systems*, Vol. 30, No. 3, pp. 337-349, March 2011
[20] Paolo Magnone, Felice Crupi, Abdelkarim Mercha, Pietro Andricciol, Hans Tuinhout and Robert J. P. Lander, “FinFET Mismatch in Subthreshold Region: Theory and Experiments” *IEEE Transactions On Electron Devices*, Vol. 57, No. 11, November 2010
[21] Ming-Hung Han, Chun-Yen Chang, Life Hung-Bin Chen, Ya-Chi Cheng, and Yung-Chun Wu, “Device and Circuit Performance Estimation of Junctionless Bulk FinFETs” *IEEE Transactions On Electron Devices,* Vol. 60, No. 6, June 2013

[22] Mayank Shrivastava, Harald Gossner, and V. Ramgopal Rao, "A Novel Drain-Extended FinFET Device for High-Voltage High-Speed Applications" *IEEE Electron Device Letters,* Vol. 33, No. 10, October 2012
[23] Takashi Matsukawa, Yongxun Liu, Shin-Ichi O'uchi, Kazuhiko Endo, Junichi Tsukada, Hiromi Yamauchi, Yuki Ishikawa, Hiroyuki Ota, Shinji Migita, Yukinori Morita, Wataru Mizubayashi, Kunihiro Sakamoto, and Meishoku Masahara, "Decomposition of On-Current Variability of nMOS FinFETs for Prediction Beyond 20 nm" *IEEE Transactions On Electron Devices,* Vol. 59, No. 8, pp. 2003-2010, August 2012
[24] F. Crupi, M. Alioto, J. Franco, P. Magnone, M. Togo, N. Horiguchi, and G. Groeseneken, "Understanding the Basic Advantages of Bulk FinFETs for Sub- and Near-Threshold Logic Circuits From Device Measurements" *IEEE Transactions On Circuits And Systems—II: Express Briefs*, Vol. 59, No. 7, July 2012
[25] Ajay N. Bhoj, and Niraj K. Jha, "Design of Logic Gates and Flip-Flops in High-performance FinFET Technology" *IEEE Transactions On Very Large Scale Integration (VlSI) Systems*, Vol. 21, No. 11, pp. 1975-1988, November 2013
[26] Cheng-Li Lin, Po-Hsiu Hsiao, Wen-Kuan Yeh, Han-Wen Liu, Syuan-Ren Yang, Yu-Ting Chen, Kun-Ming Chen, and Wen-Shiang Liao, "Effects of Fin Width on Device Performance and Reliability of Double-Gate n-Type FinFETs" *IEEE Transactions On Electron Devices,* Vol. 60, No. 11, pp. 3639-3644, November 2013
[27] Daniela Munteanu, and Jean-Luc Autran, "3-D Simulation Analysis of Bipolar Amplification in Planar Double-Gate and FinFET With Independent Gates" *IEEE Transactions On Nuclear Science,* Vol. 56, No. 4, pp. 2083-2090, August 2009